Hot Spot Aware Microchannel Cooling Add-on for Microelectronic Chips in Mobile Devices

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ABSTRACT

This work proposes an experimental microchannel solution to cool microelectronic chips with hot spots, using a non-intrusive technique. In microelectronics, approaches such as die thinning induces acute stress on cooling because it increases the hotspot phenomena and reduces chip bulk thickness aimed for microchannels. In mobile devices, the heat must be removed using limited pumping power and cooling space. Microchannels etched in the backside of the chip, usually considered as an efficient cooling solution, are impracticable on highly thinned chips. This work experimentally investigates the cooling performance of a non-invasive and hot spot aware microchannel die that is in direct fluidic contact with the backside of the chip. It also proposes a confinement-wise metric. A thermal resistance of 2.8 °C/W is achieved at heat flux of 1185 W/cm² per heat source, for a total dissipated power of 20 W and a maximum allowed temperature rise of 55 °C. Such performance is obtained with only 19.2 kPa of pressure drop and 9.4 ml/min of flow rate, making a hydraulic power of only 3 mW, representing a coefficient of performance of 6500. Therefore, backside cooling appears as a compact and low consumption solution for highly confined heat on chips for mobile applications.

KEY WORDS: hot spot, microchannels, microelectronic chips, cooling, heat transfer

NOMENCLATURE

A	Effective thermal exchange surface (m²)
A_s	Heated surface (m²)
C_p	Fluid specific heat (J/kg-K)
$\dot{Q}$	Test device dissipated power (W)
R_{cond}	Conduction thermal resistance (°C/W)
R_{conv}	Convection thermal resistance (°C/W)
R_{heat}	Temperature rise thermal resistance (°C/W)
R_{tot}	Total thermal resistance (°C/W)
T_f	Fluid temperature (°C)
T_{max}	Maximum chip temperature (°C)
T_{in}	Inlet fluid temperature (°C)
T_w	Microchannel wall temperature (°C)
$\dot{V}$	Volumetric flow rate (m³/s)
q''	Heat flux (W/m²)
h	Convection coefficient (W/m²-K)
r	Thermal resistivity (°C-m²/W)

Greek symbols

η	Fin efficiency coefficient
ρ	Fluid density (kg/m³)

INTRODUCTION

New trends such as die thinning and 3D stacking put stress on microelectronic cooling. Air cooling appears insufficient for these new microelectronics trends as it has high volumetric requirements for a limited cooling capacity [1]. Alternatively, liquid cooling can extract heat from compact chips and assemblies. As initially proposed by Tuckerman and Pease [2], microchannel cooling can accommodate high heat fluxes, so work in this area has focused mainly on cooling high power chips. Nowadays, implementations [3] mainly use embedded microchannels at the backside of the chip, due to their advantageous cooling and space requirements.

However, as discussed by Byon *et al.* [4], an important trend is die thinning, where hot spots phenomenon is exacerbated. Hot spots involve thermal non-uniformities that need to be tackled to maintain the chip integrity [5]. In addition, hot spot temperatures must be limited to acceptable levels. For mobile devices, the cooling context is different from high performance devices, as the space and available power for pumping are very limited. Although hot spots can be present, the total heat to dissipate remains moderate at ~5 W in current chips [6].

Solutions are proposed to manage both the temperature uniformity and the maximum temperature of the hot spots. Sharma *et al.* [7] propose an embedded microchannel local cooling approach by using smaller microchannels over the hot spots. Madhour *et al.* [8] propose a concept of microchannels on an additional stacked die, which in their case is the upper die in a 3D stacking. However, such embedded solutions are impracticable if the die thickness is too small for microchannel etching. Indeed, some chips, being designed for a specific application, can be considered *a posteriori* for another use and thermal requirements. If the chip is already thinned, the use of an add-on solution is preferable to direct etching. As the next generations of mobile device chips could reach 15 W, is there a solution to cool them in a hot spot context with limited space and pumping power, by avoiding to alter the chips?

This work proposes a single die layer containing microchannel patterns adapted for the hot spots and providing direct fluidic contact with the backside of the microelectronics chip. It aims at developing a prototype with the following properties:

- Chip temperature rise kept ≤ 55 °C for a 15 W heat generation;
- Better cooling than an added microchannel reference die using only thermal interface material for stacking;
- Cooling die and test chip total thickness must be kept below 1 mm.

Another objective is to develop a relevant way of comparing the test chips when the heat sources are highly confined. In the

following, the details of the test chip representing a logic chip for mobile devices are first described. It is followed by the process flow to build and assemble the test chip and the cooling prototype. The thermal resistance testing method is then presented before the results are analyzed. Finally, a new metric is proposed for highly confined heat source cooling.

METHODOLOGY

The approach aims at experimentally comparing two microchannel cooling configurations that provide indirect and direct fluid contact to the chip (fig. 1). The first consists of a standard microchannel cold plate assembled with a thermal interface material to the chip. It offers a more important thickness of bulk Si for heat spreading. The second consists in assembling open microchannels directly to the chip backside, which offers a direct fluidic contact with the chip without etching it. A custom thermal test chip with heaters and temperature measurement is used for heat generation. For such a comparison, the total thermal resistance, R_{tot}, between the heat sources on the chip and the fluidic inlet temperature, respectively T_{max} and T_{in}, are used and expressed as:

$$R_{tot} = \frac{T_{max} - T_{in}}{\dot{Q}} \quad (1)$$

where $\dot{Q}$ is the dissipated power from a test chip.

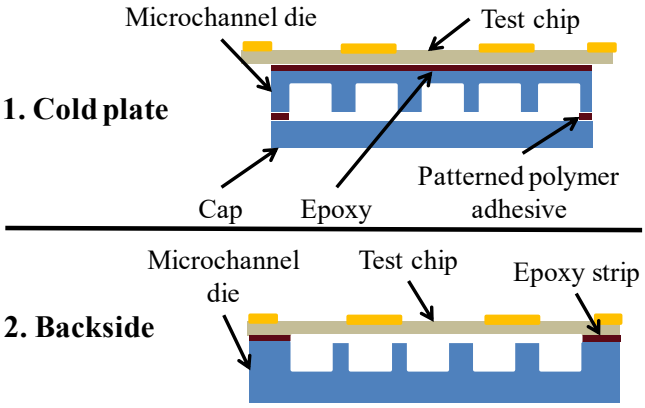

Fig. 1 Cold plate and backside stacking cross-sections

Isolating the thermal resistance contributions

The total thermal resistance can be decomposed into three components identified by Tuckerman & Pease [2], which are:

Conduction resistance R_{cond}: the heat generated on a chip must first cross the solid components between the heat source and the fluid. It is defined in 1D as:

$$R_{cond} = \frac{T_{max} - T_w}{\dot{Q}} \quad (2)$$

where T_w is the temperature at the microchannel walls.

Convection resistance R_{conv}: this resistance is present at the interface between the channels walls and the cooling fluid:

$$R_{conv} = \frac{T_w - T_f}{\dot{Q}} = \frac{1}{\eta h A} \quad (3)$$

where T_f is the fluid temperature, h is the convection coefficient and A is the effective thermal exchange surface. The term η is a fin efficiency coefficient associated to the heat conduction in the vertical walls and takes into account the uneven heat distribution on the microchannel walls.

Heat resistance R_{heat}: the temperature rises in the fluid as it goes through the microchannels. It is expressed by a thermal resistance from its energy balance equation:

$$R_{heat} = \frac{T_{out} - T_{in}}{\dot{Q}} = \frac{1}{\rho \dot{V} C_p} \quad (4)$$

where ρ is the fluid density, T_{out} is the outlet temperature, $\dot{V}$ is the volumetric flow rate and C_p is the fluid specific heat.

A spreading resistance is added to those three resistances. It consists of the lateral thermal resistance in the solid part when a heat source is confined compared to the cooling surface. Although originating in the solid part of the heat path, it affects the lateral heat distribution and not only R_{cond}, but also R_{conv} and R_{heat}, as the microchannels are unequally exploited. This issue has been discussed in Collin *et al.* [9].

DEVICE FABRICATION

A test chip is first developed in order to thermally reproduce the Wide I/O chip from Dutoit *et al.* [10]. This chip is a 300 µm thick Si die of 8.55 x 8.56 mm². Heat sources are fabricated as metallic serpentine patterns for ohmic heating, which also serve at RTDs for temperature measurement. This chip is presented in fig. 2 and the process is detailed in Collin *et al.* [11].

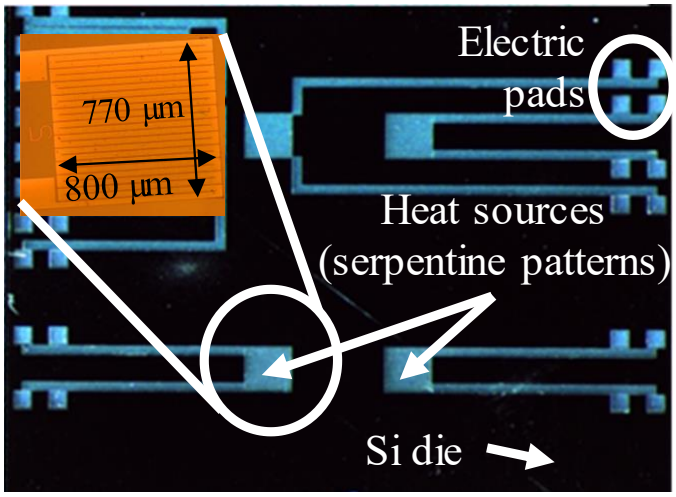

Fig. 2 Thermal test chip with hot spot heaters and temperature measurements, simulating heat generation of the 3DNoC [10]

The microchannels are processed by deep reactive ion etching (DRIE) on the surface of a 200 mm Si wafer. For the backside configuration however, it is done on a thinned bare wafer that is eventually stacked on the chips. The details of the microchannel process are available in Collin *et al.* [11]. A range of microchannel configurations are fabricated, with various array sizes and dimensions. The tested microchannel layouts and their common dimensions are presented in fig. 3, while their dimensions are available in table 1.

Table 1 Layout dimensions

Layout	Channel width (µm)	Wall width (µm)
D	-	-
R	100	100
HM	50	50
HLM	100	50
HLL	100	100
F	150 fins length: 100	50

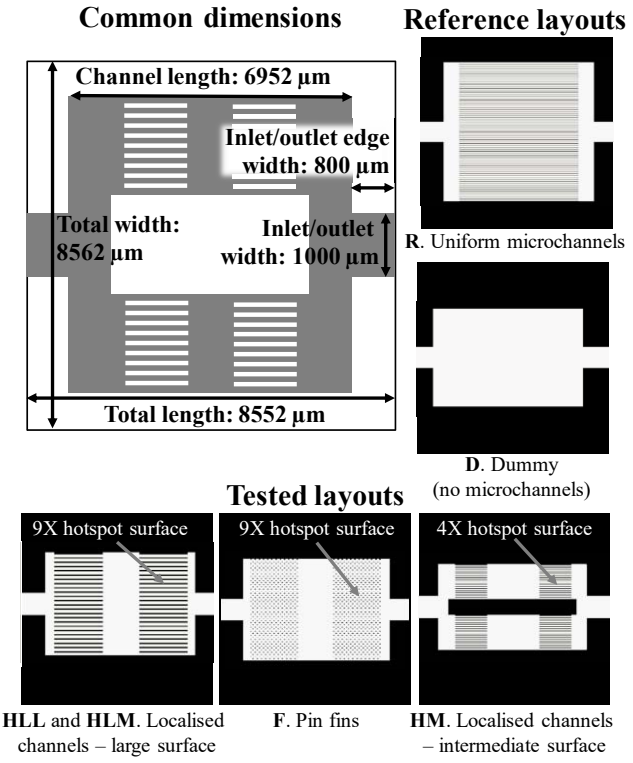

Fig. 3 Microchannel die layouts and common dimensions

Assembly and packaging

Once the microchannels are fabricated, they must be assembled with the test chip according to the configuration presented in fig. 1. The cold plate configuration consists of a microchannel die picked-and-placed on a thinned cap wafer, where a layer of SiNR polymer adhesive has previously been patterned by photolithography. A second pick-and-pace operation fixes the test chips on the backside of the microchannel die. The cap wafer is finally diced.

The backside configuration is made by etching the microchannels into a wafer. The face opposite to the microchannels is thinned from 725 µm to 425 µm. The test chips are pick-and-placed in a chip-to-wafer approach on the microchannel face, as presented in figure 6. The microchannel dies are finally diced to the chip dimensions.

The packaging requires fluidic and electrical interconnections for testing. Capillary tubes of 1 mm inner diameters are fixed on the device sides for inlet and outlet fluidic interconnections. The device is then placed on an adapted 28 pins dual inline package (DIL28) and electrical connection are formed by wire bonding, as shown in fig. 5. The air gaps above and below the device offers negligible heat paths compared to the liquid cooling. Therefore, the only significant chip heat sink are the microchannels [11].

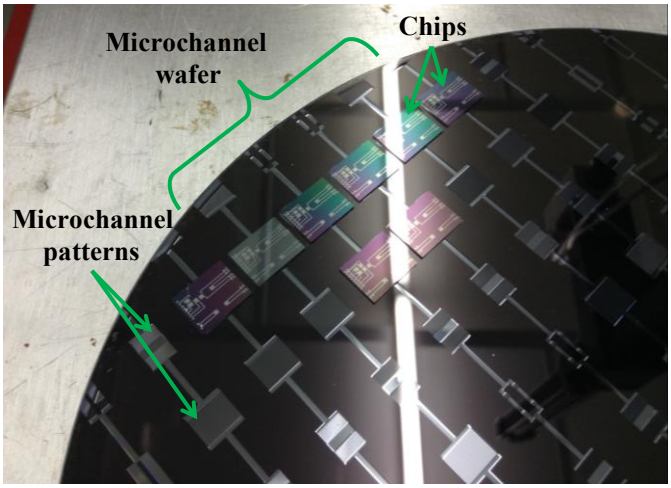

Fig. 4 Microchannel patterns on a 200 mm pick-and-place assembled with test chips (backside configuration)

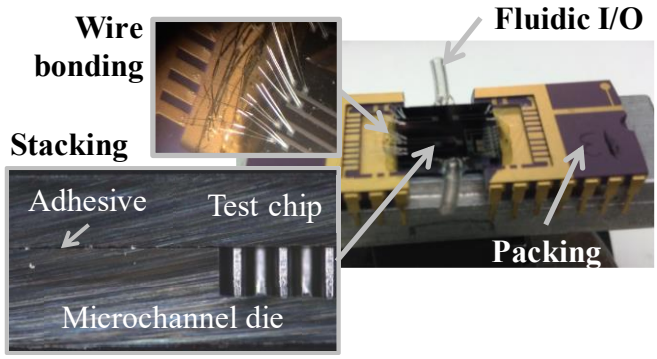

Fig. 5 Microfluidic and electronic packaging for tested device

Apparatus

First, a test bench is developed in order to control and monitor the metrics related to the performances. Many studies [7, 12, 13] propose relevant test benches, from which the one from Collin *et al.* [11] is inspired and used for the present study. This test bench is presented in fig. 6.

Then, a group of Bartels Mp-6 micropumps is placed in the closed loop circuit and the flow rate is controlled through a microcontroller. A Sensirion SLS-1500 flow meter is placed in series in the circuit in order to monitor the fluid flow rate.

The pressure drop and temperature rise in the fluid across the device are monitored thanks to the temperature and pressure sensors located before and after the chip. Four independent electric circuits feed the heat sources and temperature measurements are done using the thermoresistive properties of the serpentine patterns, with a four-point measurement. The power for each heat source is also obtained from the measured current and voltage drop.

To measure a thermal resistance of a device, multiple power steps are applied on the heat sources. At each step, a similar power is applied on each heater and sufficient time is allowed to reach the steady-state. By repeating this procedure for

different power steps, it is possible to obtain a power-temperature correlation.

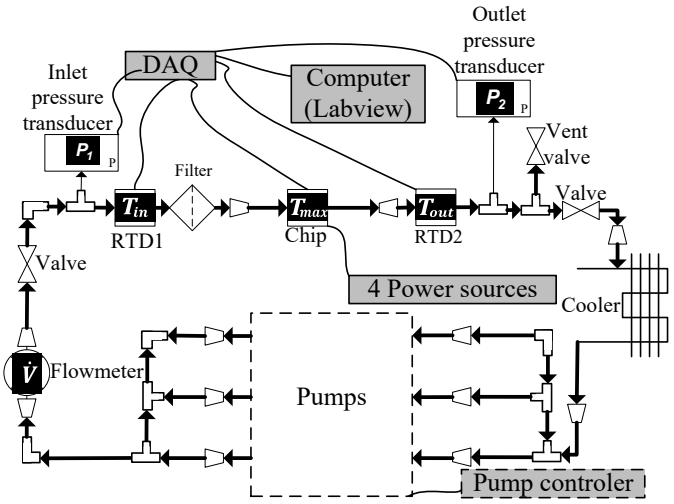

Fig. 6 Fluidic pattern of the test bench

CHARACTERIZATION RESULTS

The devices from both configurations are tested and the performances of the devices are evaluated based on their configuration and microchannel layouts. As presented in fig. 7 for available devices successfully patterned and stacked, the most influent factor is the presence of microchannels or pin fins in the cold plate configuration. Indeed, the device with the most significant thermal resistance is 2.1 °C/W below the device with a single cavity for the same electrical pumping power. It is followed by the stacking, where the backside configuration systematically offers better cooling for every microchannel layout. In average, the backside devices offers 7 to 20 % less thermal resistance than the cold plate configuration. The microchannel layout has a minor effect in the context of this research, the variation being below 8 % with the average cooling for each stacking configuration. The weak layout influence over the backside configuration could origin from the lack of thermal bonding between the test chip and the microchannels or the pin fins. In such case, their impact on the boundary layers would be their only influence over R_{tot}.

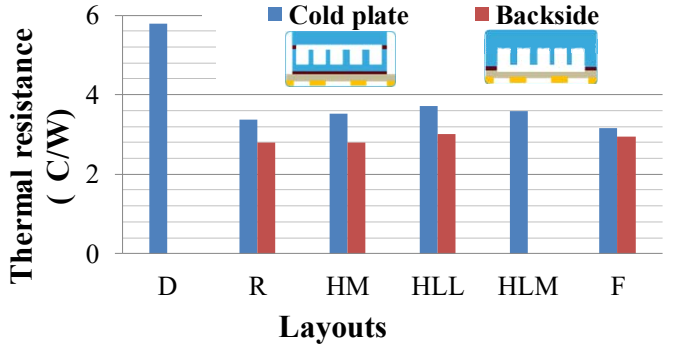

Fig. 7 Summary of the thermal performance reached according to the stacking and the microchannel layout

It can be concluded that a thermal resistance of 2.8 °C/W can be achieved with a pressure drop of 19.2 kPa and a flow rate of 9.4 ml/min, representing an hydraulic power of 3 mW with both the R and the HM cooling layouts in backside configuration. In addition to cooling performance, the devices with backside cooling have an overall thickness of 0.66 mm, excluding the capillaries, compared to 1.39 mm for the devices in a cold plate configuration.

DISCUSSION

The results presented in this section are analyzed with a larger scope, starting by comparing the obtained results to the literature. The relevance of the comparison metrics is also analyzed in order to associate them properly to the hot spot cooling context. A discussion on the microchannel cooling design closes this section.

Constriction metric

A conventional way of comparing the thermal performance is to observe the thermal resistance of a device as a function of the flow rate [12, 14]. In such context, the prototype from this study does not offer a competitive thermal resistance, but uses a lower flow rate. For instance, Tuckerman and Pease [2] reached 0.09 °C/W at 516 ml/min with regular straight microchannels and Biswal *et al.* [12] reached 3.0 °C/W at 60 ml/min to cool a heat source representing only 4 % of the cooling surface. So, the comparison is not conclusive for the prototype, as a reduced flow rate could offer similar or better results from the other studies.

Although flow rate is commonly used as a metric, the hydraulic power would be more adapted for comparison by considering both the pressure drop and the flow rate. This metric is closely related to the heat power to dissipate, so the ratio of hydraulic power over heating power is a relevant one to minimize, as proposed by some authors [7].

In addition, confined heat generation on a chip adds heat spreading thermal resistances to the model, making it harder to reduce the global thermal resistance [9]. So, it would be relevant to include such confinement in the performance metric used. Here, we define *thermal resistivity*, r, as:

$$r = R_{tot} * A_s = \frac{T_{max} - T_{inlet}}{q"} \qquad (5)$$

where A_s is the heated surface and q" is the hot spot heat flux. This way, this metric includes the confinement level and highlights the difficulty to cool locally high heat fluxes. In addition, the coefficient of performance (COP), representing the heated power over the hydraulic power is used. The higher its value the more efficient is the cooling system. For the thermal resistivity, a low value due to constriction means that low R_{tot} values could be difficult to reach. Indeed, the resistance to heat spreading coming from the heat source constriction increases R_{tot}. Tuckerman and Pease [2] obtained 0.09 °C-cm²/W at a COP of 430, while Biswal *et al.* [7], reached 0.12 °C-m²/W for a COP of 65. In comparison, the present prototype offers 0.067 °C-cm²/W with a COP of 6500, which indicates the higher level of constriction from the heat source to be cooled with a better efficiency. The significant heat flux of 1185 W/cm² and the small heated area explains why the resistivity is so low.

Thermal resistance analysis: R_{heat}, R_{conv}, R_{cond}

The results show that the backside cooling has a lower thermal resistance than the cold plate configuration. This

suggests that R_{cond} can still be significant for the cold plate configurations.

Except for the D layout, the low R_{tot} variation from the microchannel layout suggests that the R_{conv} is small in the cold plate configuration compared to the other resistances. This means that the exchange surface is sufficiently large to avoid being a sensitive parameter for R_{tot} in such ranges. However, the significantly higher thermal resistance from the cavity layout (D), shows that putting microchannels or fins remains relevant in this context, at least for the cold plate configuration.

CONCLUSION

The aim of this study was to propose a cooling solution to manage localised hot spots on chip without impacting the chip fabrication process. For this, an experimental add-on cooling approach with direct fluidic contact at the back side of the chip is investigated. The developed prototype showed a significantly reduced thermal resistance and total thickness compared to a cold plate configuration.

It showed that the different tested microchannels or fin layouts only had a secondary role compared to the stacking configurations in the global thermal performance. Only the cavity without microchannels showed significantly higher thermal resistance for the cold plate configuration.

A new metric, presented as a thermal resistivity, has been developed in order to include the heat flow rate produced by the heat sources. Such metric is complementary to the thermal resistance, by including the heat confinement level.

In this context, the best developed prototypes showed a modest thermal resistance of 2.8 °C/W, but with a heat flux from heat sources as high as 1185 W/cm² and presented one of the best thermal resistivity in literature. With such heat flux, chips generating up to 20 W can limit their temperature rise to 55 °C/W with a pressure drop of 19.2 kPa and a flow rate of 9.4 ml/min. This represents an hydraulic power of 3 mW and a coefficient of performance of 6500. In addition, the total height of both the microchannels and the chip only reached 0.66 mm. At the light of these results, it is possible to cool a 15 W chip, with is a highly confined heat source and limited cooling space and pumping power.

The proposed solution is also adapted as a post-fabrication solution. So, even in the case where a highly thinned chip needs cooling in an specific application, the backside approach can provide a solution without modifying the process flow map.

Future works should focus on the need for cooling system being functional at temperatures below 0 °C, which involves compromises on the fluid properties. In the present scenario, water was used for a better comparison with other solutions from the literature. However, fluids such as the ethylene glycol and water mix should be considered for sub-zero temperatures. Its significantly higher viscosity makes the low velocity in small channels even more appealing. Layout designs could be of more importance in such context. An optimization method able to manage the numerous design parameters should be established in order to find the most important aspects to consider while designing.

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