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MICROCHANNEL DESIGN STUDY FOR 3D MICROELECTRONICS COOLING USING A HYBRID ANALYTICAL AND FINITE ELEMENT METHOD

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ABSTRACT

For microelectronics cooling, microchannels are a potential solution to ensure reliability without sacrificing compactness, as they require relatively small space to remove high heat fluxes compared to air cooling. However, designing microchannels is a complex task where simulation models become a forefront tool to investigate and propose new solutions to increase the chip thermal performances with minimal impact on other aspects.

This work evaluates numerically the impact of microchannel cooling in a standalone chip and a 3D assembly of two stacked chips with localized heat sources. To do so, a modeling approach was developed to combine finite element modeling of conduction in the chip using commercial software with analytical relations to capture the heat transfer and fluid flow in the microchannels. This approach leverages the multiphysics and post-processing capabilities of commercial software, but avoids the extensive discretization that would normally be required in microchannels with full finite element modeling. The study shows that increasing the flow rate is not as beneficial as increasing the number of channels (with constant total cross-section area). The effect of heat spreading was also found to be critical, favoring thicker dies. When switching to 3D chip configuration, the interdie underfill layer significantly increases the total thermal resistance and must be considered for thermal design. This effect can be significantly alleviated by increasing the interdie thermal conductivity through adding copper micropillars.

INTRODUCTION

The microelectronics sector is facing many challenges to produce smaller and more powerful computing chips. Thermal management is one of those, which comes from new developments such as chip stacking (3D chips) and increasing the computing power. In addition to increased cooling needs, the mobile device market tends to reduce the space available for heat dissipation. In this context, conventional air heat sinks are inadequate and alternative compact and high heat flux cooling approaches are required. Liquid cooling with microchannels is an approach that offers both compactness and cooling performance that can be well above air cooling [1, 2].

Although microchannel cooling has been shown to be promising for over 30 years, challenges remain for their design and integration with microelectronics. A major challenge to establish a design is the non-uniformity of the chip heat sources [3]. The adaptation of a cooling solution to a specific chip requires knowledge of its heat paths and power source characteristics. Much work has been dedicated to trace the thermal layout of microelectronic chips [4-6], providing valuable data for thermal management. It has shown that spreading due to lateral conduction from the hot spots and through 3D stacks must be taken into account to properly evaluate the maximum chip temperature. Also essential is the understanding of microchannel flows and heat transfer. This area has matured to the point where analytical tools to design microchannels are now available [7].

However, it is essential to merge both the chip thermal conduction model and the fluidic cooling system together to

take into account their coupled effects. This aspect is especially relevant when designing the cooling system to efficiently use the pumping power. Reducing pumping power helps to both reduce the device needs in power and space.

Relatively simple analytical models were proposed to define the chip thermal scheme layout [8-10]. Although convenient for uniform planar properties and heat source, they are rapidly limited when comes time to simulate the heat spreading on complex structures. Simulating heat spreading is critical as it generally has an important impact on the chip thermal resistances [8]. Some authors, such as Bagnall *et al.* [11], pushed the analytical approach up to more complex 3D configurations, including multiple heat sources, orthotropic layers and thermal spreading on multiple stacked layers. However, such models do not include multiple materials in a single layer or a two sided heat spreading for the heat sources. The complex geometry of true 3D integrated circuit (3DIC) products emphasizes the limitations of such analytical models.

The use of discretized numerical simulations for fluid mechanics and heat transfer in chips with microchannels requires important computing resources as the whole flow and structure need to be meshed. In addition, a much finer mesh is required for the fluid in the vicinity of the walls in order to include the thermal gradients. To increase computational power, alternative approaches were proposed, such as developing Graphic processing unit (GPU) computing adapted models [14]. No matter the performance, simulating the microchannel flow is generally resource consuming and the detailed local flow quantities are not so relevant. In many cases, the convection coefficient and mean fluid temperature along the microchannel would suffice as boundary conditions on a 3D conduction model to meet the simulation needs.

Numerical models dedicated to 3D chip have therefore been developed. They generally represent the chip and microchannels by a thermal resistance network through finite difference elements [12, 13] and are more adapted to tackle the conjugate heat transfer in 3D chips. They showed good accuracy compared to full 3D finite-element (FEM) or experimental tests for a fraction of the computing time, which makes them a valuable asset for thermal study in early-design phases.

A similar approach is adopted in this work, but by combining commercial finite element software to model conduction in the chip with 1D analytical relations to represent the flow and convective heat transfer along the microchannels.

In comparison with other similar models, the use of commercial software readily allows multiphysics studies, such as thermomechanical behavior due to microchannel cooling, as well as the use of extensive post-processing capabilities. This model is used to gain insight on the design parameters for microchannels embedded on both a standalone and a 3D chip.

In this paper, the proposed conjugate heat transfer method is first described. Then, the modeling approach for a standalone chip and a 3D stacked chip are presented. A parametric analysis is done on both the standalone chip and the 3D models. Finally, relevance of the method is discussed.

Thermal resistances

Before detailing the analytical-numerical model structure, the relation between the thermal resistances is first studied to both understand the model itself and interpret the results. As shown in Fig. 1, heat goes through different thermal resistances as it flows from the heat source to the cooling fluid and essentially corresponds to Tuckerman *et al.* approach [2].

Conduction resistance

The first resistance, R_{cond}, represents the conductive resistance from the chip layers and fins before reaching the microchannel walls. This resistance includes lateral heat spreading, which also affects both subsequent resistances due to new parallel thermal paths in the network, presented below the microchannels on both sides of Fig. 1. More spreading would mean a larger apparent convection surface for the subsequent thermal resistances. The term "apparent" refers here to the fluid or material crossed by a significant part of the total heat flux $\dot{Q}$. The conduction resistance R_{cond} for a single layer, without spreading, is obtained from Fourier's law:

$$R_{cond} = \frac{t}{kA_{cond}} = \frac{T_{source} - T_{wall}}{\dot{Q}} \quad (1)$$

where t represents the different chip layer thicknesses, A_{cond} is the apparent surface crossed by the flux, T_{source} is the source temperature and k is for the layers thermal conductivity. This simple relation reveals to be more complex when a closer look is taken on its variables. First, k is dependent from the various materials in the chip, meaning that its value changes in the three space axes. Temperature can also influence significantly k. So, k is a discontinuous temperature dependent variable. Second, the heat flux density varies spatially in the three dimensions due to thermal spreading, making A_{cond} a variable in the need of definition. In short, it is unlikely to rely on simple 1D expressions to solve such complex 3D model and thereof, it justifies relying on numerical simulation for this part.

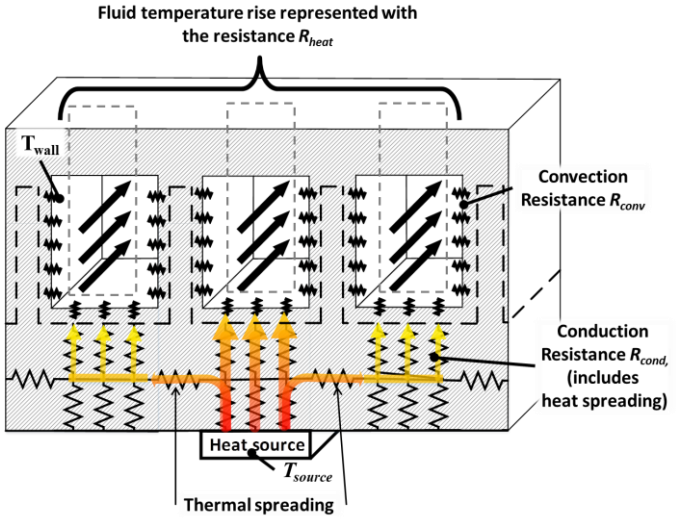

Fig. 1– Heat resistances in microchannels

Convection resistance

The second resistance is the convection happening at the solid-liquid interface, represented from Newton's law of cooling:

$$R_{conv} = \frac{1}{h_{micro} A_{conv}} = \frac{T_{wall} - T_{fluid}}{\dot{Q}_{channel}} \quad (2)$$

where A_{conv} is the microchannel surface, $\dot{Q}_{channel}$ is the heat flux crossing the walls and absorbed by the fluid, h_{micro} is the convection coefficient and T_{wall} is the surface averaged wall temperature, as the temperature varies along the two wall axes. Enhancing the spreading in the chip allows a larger apparent surface A_{conv} of the microchannels walls to evacuate heat in the fluid, consequently reducing R_{conv}. Such phenomenon highlights the need to couple the conduction with the convection in order to take the advantage of the spreading for the convection resistance.

Temperature rise in the fluid

The last resistance represents the fluid temperature rise along the channel, taking T_{inlet} as the fluid temperature reference. This fluid resistance R_{heat} is directly linked to the fluid properties and flow rate, obtained from energy balance:

$$R_{heat} = \frac{T_{outlet} - T_{inlet}}{\dot{Q}_{channel}} = \frac{1}{\rho \dot{V} C_p} \quad (3)$$

where T_{inlet} and T_{outlet} are respectively the microchannel inlet and outlet temperatures, ρ is the fluid density C_p is the fluid heat capacity and $\dot{V}$ is the total apparent volumetric flow rate. The conversion of the fluid temperature rise in R_{heat} involves that T_{fluid} can be replaced by T_{inlet} for the calculation of R_{conv}, which eases its computation.

However, if the heat flux is localized on a small zone of the chip, not all the channels would be used and the total apparent flow rate would only be a fraction of the real total flow rate. So, the spreading in the chip also acts on R_{heat} by increasing the apparent number of channels involved in the heat exchange.

The whole circuit is in series, as represented by:

$$R_{tot} = R_{conv} + R_{cond} + R_{heat} \quad (4)$$

where R_{tot} is the total thermal resistance of the heat path. This means that the thermal resistances are summed to obtain the global thermal resistance. If some resistances are important compared to others, they must be reduced to achieve a notable change of the maximum chip temperature. The analytical-numerical model can be used to evaluate the most sensitive parameters and guide the reduction in the total thermal resistance.

MODELING

The numerical model is the tool from which the thermal analysis is to be undertaken. The section fist describes the iterative process used to solve the model. Then, the geometrical models to simulate respectively the standalone and the 3D chip are presented. Next, the microchannels representation is described, followed by the accuracy and convergence aspects.

Conjugate modeling approach

The method consists in producing a simulation model of heat transfer where conduction in the solids is modeled in 3D by FEM and microchannels walls are convective boundaries. Those boundaries are subdivided into several sections among the length axis of the microchannels. Each section is characterized by a specific temperature and heat flux.

The fluid temperature in the microchannels will vary from the inlet to the outlet, depending on the heat rejected (or collected) in each section. The mean fluid temperatures are found using an iterative approach based on energy balance for each section of the channel, using the wall temperature from the FEM model. An iterative process, represented in Fig. 2, is used to converge to the actual wall temperatures and heat fluxes.

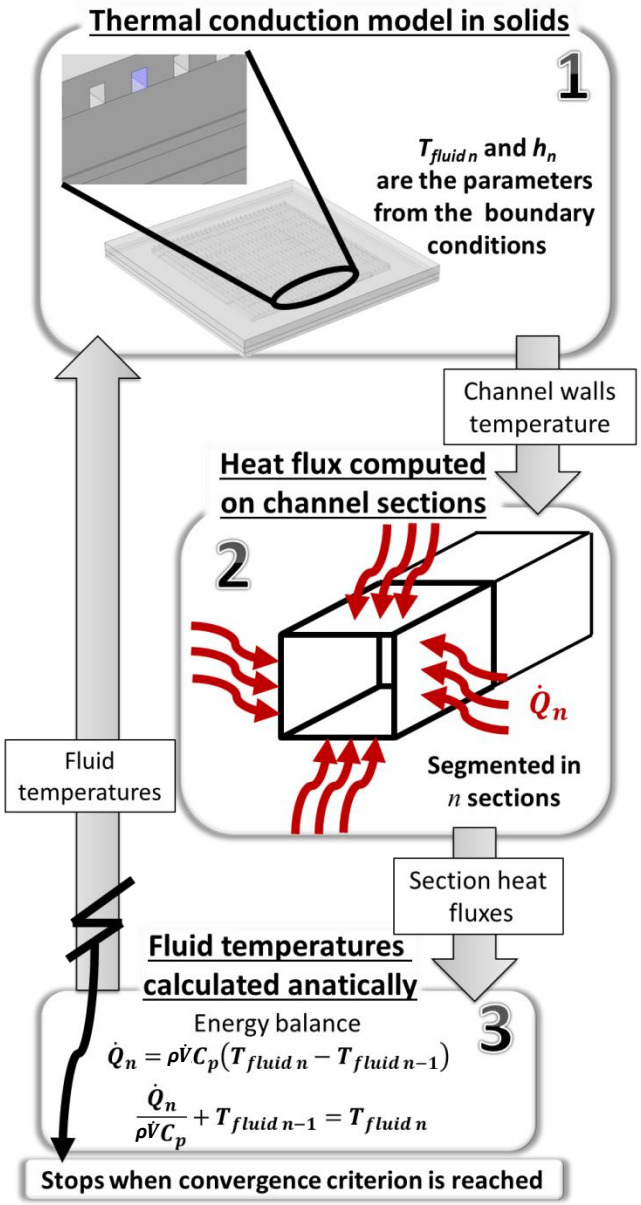

Fig. 2 – Overall modeling approach combining finite elements modeling with analytical relations

Configurations: standalone chip and 3D chip

The first step is to create the numerical model, representing a standalone chip [15], as shown in Fig. 3. Those chips are not simply a stack of different layers but also include many small components (e.g. electrical interconnections) that would be unpractical to discretize. So, those components are homogenized with the material in their surroundings using the method proposed by de Crécy [16]. The planar and normal thermal conductivities are determined independently in order to represent the thermal behavior in those areas. Microchannels are located in the Si die up to the Si-molding junction. The model geometry, including the homogenized zones is presented in Fig. 4. Table 1 presents a summary of the thermal conductivities and dimensions used. The logic die thermal conductivity is approximated by a power law based on empirical results [17].

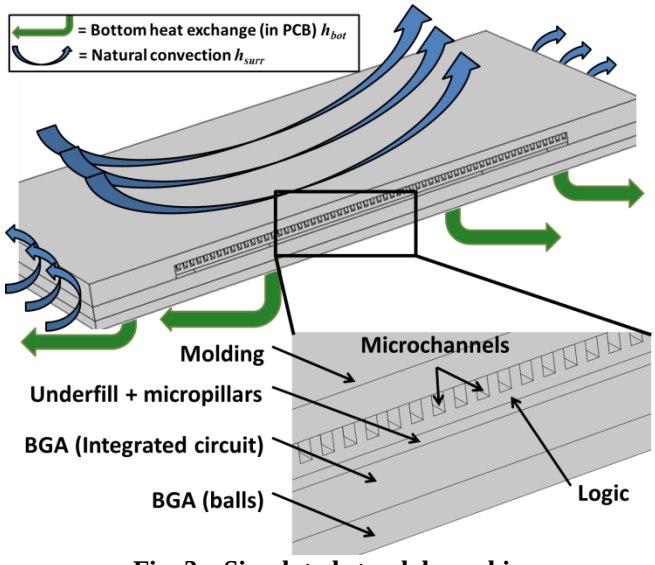

Fig. 3 – Simulated standalone chip

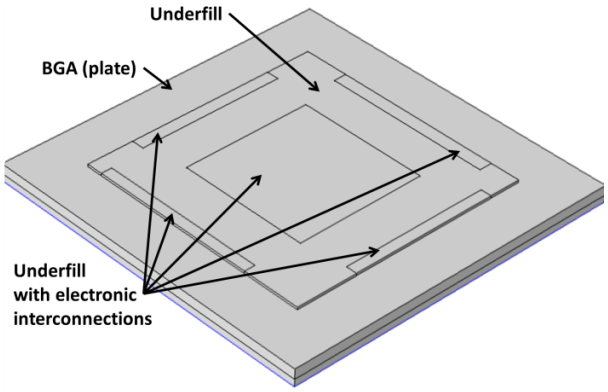

Fig. 4 –Simulated standalone chip showing the layer below logic die

Table 1 – Chip layer dimensions and thermal conductivities

Layer	Thermal Conductivity (W/m-K)		Thickness (µm)	Sides (mm)
-	Planar	Normal	-	-
Molding	0.88		200 (above logic)	12 X 12
Si die	161 952*$T^{-1.225}$		200	8.5 X 8.5
Underfill (polymer)	1.5		70	8.5 X 8.5
*Underfill (polymer+pillars)	1.9	3.5	70	
BGA (substrate)	92	0.6	288	12 X 12
BGA (balls array)	0.7	8	210	

T: Temperature [K]
*: Homogenized zone

The boundary conditions surrounding the chip are natural convection with a convection coefficient estimated to h_{surr}=10 W/m²K [15]. The bottom of the model is normally linked to a Printed Circuit Board (PCB), which allows important lateral heat spreading, with an equivalent convection coefficient estimated to h_{bot}=570 W/m²K [15].

A second configuration will also be evaluated, consisting of a 3D stacked chip. It is similar to the standalone chip simulation, where the added elements are presented in Fig. 5 and Fig. 6. The heat sources have the same pattern than the standalone chip and are exclusively located on the downward face of the bottom die.

The properties of the added layers and materials are presented in Table 2. Through silicon vias (TSV) are added in the bottom die in order to electrically connect with the top die. The underlined elements from the table are those modified or added compared to the standalone chip configuration.

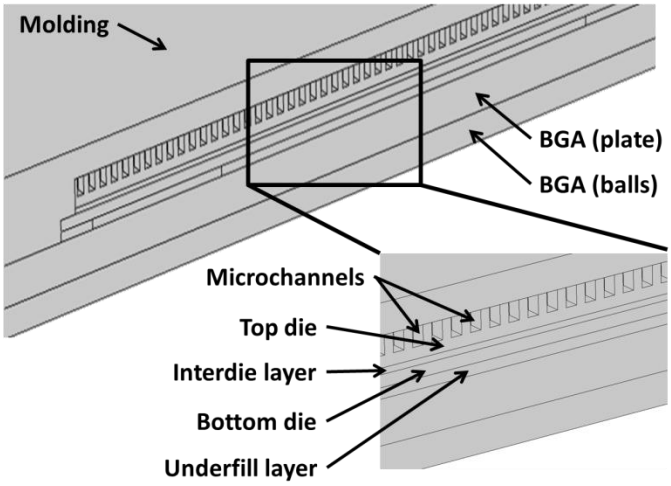

Fig. 5 – Cross-section of the 3D stacked chip assembly

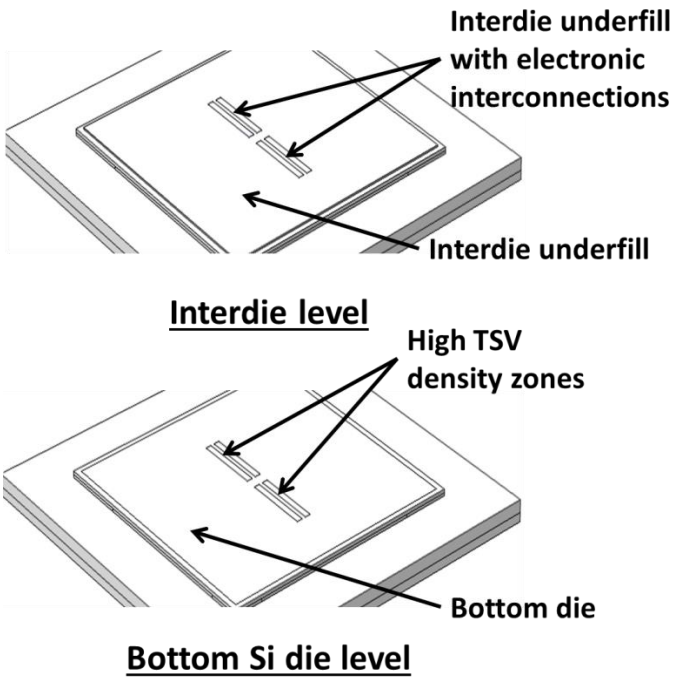

Fig. 6 – Interdie and bottom layers with homogenized zones

Table 2 – 3D Chip layer dimensions and thermal conductivities

Layer	Thermal Conductivity (W/m-K)		Thickness (µm)	Sides (mm)
-	Planar	Normal	-	-
Molding	0.88		200 (above top die)	12 X 12
Bottom die	161 952*T$^{-1.225}$		80	8.5 X 8.5
Top die			200	
*Bottom die zones with TSVs	140.4	158.6	200	4X 0.2 X 2.2
Interdie underfill	1.5		40	8.5 X 8.5
Underfill (polymer)			70	
*Interdie underfill (polymer+pillars)	1.9	3.5	40	
*Underfill (polymer+pillars)			70	
BGA (substrate)	92	0.6	288	12 X 12
BGA (balls array)	0.7	8	210	

T: Temperature [K]
*: Homogenized zone

Fluidic analytical model

Heat flux at the microchannels walls is the only unknown boundary condition to determine. For this, both the h_{micro} and the average fluid temperature in each section, T_{fluid}, need to be found. These parameters depend on the fluid flow regime and the relative developing flow length, characterized by the Reynolds number, *Re*:

$$Re = \frac{\rho V_{avg} D_h}{\mu} \quad (5)$$

where μ is the dynamic fluid viscosity and V_{avg} is the fluid average speed. D_h is the microchannel hydraulic diameter, represented by:

$$D_h = \frac{2 w_c h_c}{w_c + h_c} \quad (6)$$

where w_c and h_c are respectively the microchannels width and height. Table 4 presents the *Re* for all the flows to be evaluated. It shows that the laminar flow condition is respected for the whole set of simulation, since *Re*<2000.

To evaluate if the developing length, L_e, of the fluid in the microchannels is negligible or not, the relation proposed by Shah and London [18] in the case of a laminar flow is used:

$$L_e \approx \left(0.06 + 0.07\frac{1}{\alpha} - 0.04\left(\frac{1}{\alpha}\right)^2\right) Re D_h \quad (7)$$

where α is the largest ratio between w_{chan}/h_{chan} and h_{chan}/w_{chan}. Then, L_e is divided by the microchannel length L_{tot} to find the relative developing length:

$$L_{e\,rel} = L_e / L_{tot} \quad (8)$$

If the developing length L_e is below 10 % of the total microchannel length, the flow can be assumed to be fully developed. In this case, the convective heat transfer can be determined for rectangular channels by Nusselt number (*Nu*) correlations such as the one proposed by Brunschwiler *et al.* [19]:

$$Nu_\infty = 3 + \frac{1}{\frac{1}{h_c/w_c} + 0.2} \quad (9)$$

with h_{micro} being determined with:

$$h_{micro} = \frac{k_f Nu}{D_h} \quad (10)$$

where k_f is the fluid thermal conductivity. As shown in Table 4, the developing length L_e in the range of interest is generally below 10 % of the total microchannel length, so the flow can be assumed developed. The developing length criterion is however not fulfilled for the flow rates of 3.75 and 7.5 cm³/s. This means that some reserves should be taken, as h_{conv} is underestimated in the entrance region and the total ΔP would also be larger.

Determining sections properties

For laminar and fully-developed flow, h_{micro} can be defined only by geometrical and fluid properties, which consequently allows finding the fluid temperature in each section. As the fluid properties are coupled with the heat distribution in the chip, an iterative process is used. The iterative process starts by arbitrarily assuming the inlet temperature in all sections of the microchannels to initiate the simulation. At this point, the heat flow integration is done on the four microchannel walls of every section in order to obtain the incoming flux in each section $\dot{Q}_{sect}$. For any section *n*, the average fluid temperature $T_{sect\ n}$ is adjusted according to the energy balance on a section

and the incoming fluid temperature from the previous section $T_{inter\ n-1}$. In other words, $T_{inter\ n-1}$ is the temperature outlet from section n-1 and is used as the temperature inlet for section n. For the sections in contact with the microchannel inlet, T_{inlet} replaces $T_{inter\ n-1}$. Only $\dot{Q}_{sect}/2$ is used to get T_{sect} from $T_{inter\ n-1}$. Fig. 7 illustrates the heat fluxes and temperatures among the microchannels sections. The heat balance for each section and intersection are respectively represented by:

$$T_{sect\ n} = \frac{(\dot{Q}_{sect\ n}/2)}{\rho \dot{V} C_p} + T_{inter\ n-1} \tag{11}$$

$$T_{inter\ n} = \frac{(\dot{Q}_{sect\ n}/2)}{\rho \dot{V} C_p} + T_{sect\ n} \tag{12}$$

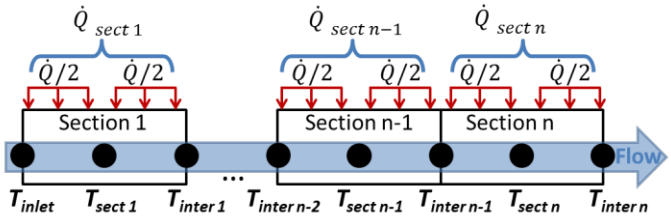

Fig. 7 – Heat fluxes and temperatures in microchannels

It is assumed that a mix of water and ethylene glycol is used in order to avoid freezing issues and that T_{inlet} is fixed at 40 °C. The fluid properties are presented in Table 3 [20].

Table 3 – Properties for a 50% ethylene-50%water solution

Property	Value	Unit
Density	1 047.3	kg/m³
Viscosity	$1.5*10^{-3}$	Pa-s
Heat capacity	3564.7	J/kg-K
Thermal conductivity	0.4	W/m-K

Pressure drop

Although not required for the thermal modeling with an incompressible fluid, the pressure drop ΔP is closely linked to the pumping power. Raising ΔP involves a reduced flow rate for the same hydraulic power P_h as it can be observed in the following formula:

$$P_h = \dot{V} \Delta P \tag{13}$$

To obtain the ΔP, the Darcy-Weisbach equation is used:

$$\Delta P = f \frac{L_{tot}}{D_h} \frac{\rho V_{avg}^2}{2} \tag{14}$$

where the f is the Darcy friction factor expressed by Shah and London [18] as:

$$f = \frac{96}{Re}\left(1 - \frac{1.3553}{\alpha} + \frac{1.9467}{\alpha^2} - \frac{1.7012}{\alpha^3} + \frac{0.9564}{\alpha^4} - \frac{0.2537}{\alpha^5}\right) \tag{15}$$

Heat management

The heating power is distributed into 8 cores of 360 X 490 µm² to represent the test-chip, as illustrated in Fig. 8. With 2 W per core, a total of 16 W needs to be removed. In order to work properly, the chip maximum temperature must be below 125 °C. Both the ambient and inlet temperatures are set at 40 °C, which is an estimate for confined air.

It would be interesting to know the minimal theoretical flow rate where the maximum allowed temperature of 125 °C is reached in the chip with the microchannels as the unique heat sink. Assuming an ideal configuration where R_{cond} and R_{conv} are negligible, it can be assumed that T_{outlet} would reach the maximum temperature of the chip. This minimal flow rate can be determined by heat balance:

$$\dot{Q}_{tot} = \rho \dot{V} C_p (T_{outlet} - T_{inlet}) \tag{16}$$

This means that any flow below 0.05 cm³/s cannot cool sufficiently the chip in those conditions. So, the maximum thermal resistance is $R_{tot\ max}$=5.3 °C/W to evacuate 16 W. The fluid flow rate is first set to 0.75 cm³/s for the reference case, meaning an average T_{outlet} of 45.7 °C. So, this flow rate is a compromise between the thermal resistance (0.36 °C/W when $\dot{V}$ is for the apparent flow rate) for a reasonable ΔP of 19.3 kPa.

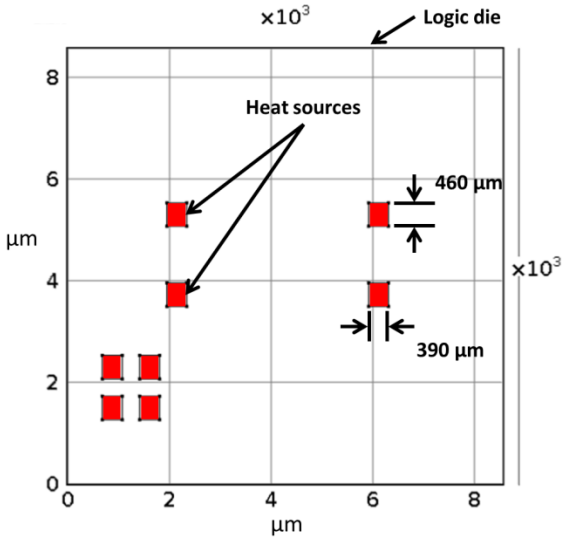

Fig. 8 – Heat sources layout on the standalone chip

Accuracy from numerical criterions

The use of an iterative numerical model involves two non-physical inaccuracies: one from the iterative process due to truncated iterations and a second from the FEM itself.

Convergence

A criterion, *lim*, is placed to stop the iterative process based on the desired level of accuracy on convergence. To stop the iterative process, the maximum relative variation between the section heat fluxes of the current iteration $\dot{Q}_i$ and previous iteration $\dot{Q}_{i-1}$ must be below *lim*:

$$\frac{\max|\dot{Q}_i - \dot{Q}_{i-1}|}{\dot{Q}_i} < lim \tag{17}$$

This way, the level of uncertainty can be set to a ratio with a negligible impact. In the study, *lim* is set to 0.05 %.

Section resolution

A sufficient amount of sections per channel must be chosen to give accurate results. Because the fluid temperatures are averaged on the channels walls, this involves an inaccuracy on the heat distribution. Such inaccuracy is reduced while the channels section length decreases, because the fluid is getting more and more discretized. To get reasonable temperature distribution in the model, 15 sections per channel are selected. At this point, the chip maximum temperature difference is below 0.2 °C compared to a discretization with 10 sections.

Heat balance

To guarantee that the whole model energetically balances, a simulation is done without natural convection. In theory, all the heat originating from the sources should be absorbed in the fluid between the inlet and outlet. The base case without external cooling has a difference of approximately 0.32 % between the input heat flux and the computed heat transported by fluid flow. So, the results show good agreement between those values.

RESULTS AND DISCUSSION

Uncooled chip

A reference case is simulated without any microchannels. In this case, the chip is exclusively cooled by the spreading below the BGA and the natural surrounding convection. In Fig. 9, the maximum temperature is well above the maximum allowed temperature of 125 °C, which clearly shows the need of a cooling solution.

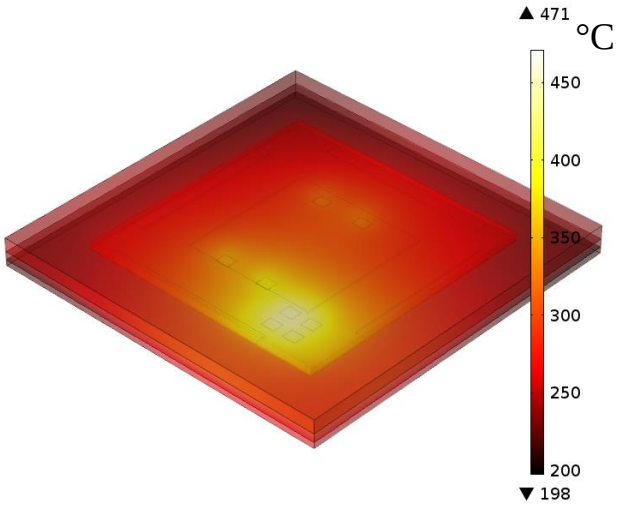

Fig. 9 – Chip simulation without microchannels, extracting heat only by natural convection and PCB heat spreading

Baseline microchannels configuration

60 microchannels are uniformly distributed in the Si die, having a height and width of respectively 125 µm and 75 µm. This configuration leaves ~68 µm for walls thickness and uses a flow rate of 0.75 cm³/s. For this configuration, the heat distribution is represented in Fig. 10, where T_{max} rises to 97 °C, satisfying the temperature criterion. A total thermal resistance of R_{tot}=3.6 °C/W can be extracted from the simulation results from the equation:

$$R_{tot} = \frac{T_{max} - T_{inlet}}{\dot{Q}} \quad (18)$$

Neglecting the temperature dependent properties for the Si and the fluid, the correlation between Q and ΔT is proportional. This means that such a configuration would allow 23.8 W for T_{max}=125 °C. The maximum allowed power is one of the relevant criterions indicating how much computing power and functionalities can be integrated to the chip.

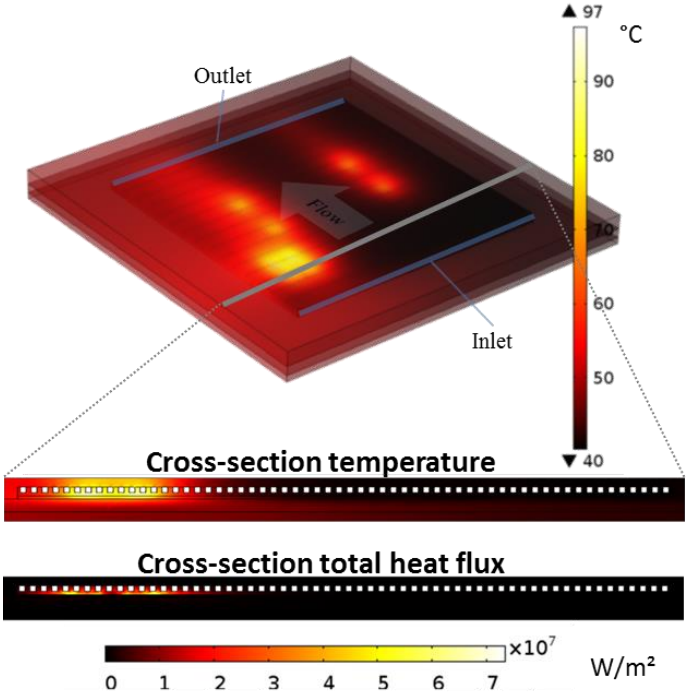

Fig. 10 – Microchannels simulation dissipating 16 W in a flip-chip with 60 microchannels of 125 µm deep and 75 µm wide (flow rate 0.75 cm³/s)

Standalone chip application

To increase the cooling potential, one can increase the flow rate in order to lower the fluid temperature raise and so, R_{heat}, in the microchannels. However, if the fluid temperature raise is already small, increasing the flow rate will only have little impact on the maximum dissipating power at the price of important pumping power. Fig. 11 illustrates the estimated maximum dissipating power possible according to the fluid flow rate. The trend shows a horizontal asymptote due to the fact that R_{cond} and R_{conv} are kept constant and that only R_{heat} is reduced to negligible values. At 7.5 cm³/s, assuming R_{heat}~0 °C/W, the residual resistance combining R_{cond}+R_{conv} represents a considerable resistance of 3.6 °C/W. This highlights the fact that efforts must be first applied on the most resistive part of the resistance circuit. This heat removal is somewhat modest compared to the 790 W/cm² extracted on a 1 cm² Si die [2], but stress the importance of dealing with very high density heat sources.

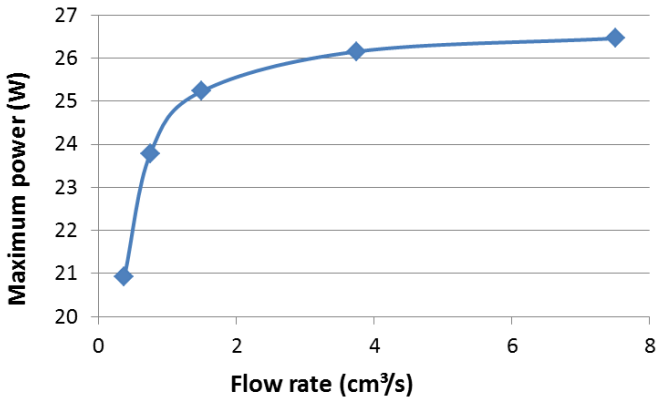

Fig. 11 – Maximum power admissible to reach a maximum temperature of 125 °C according to fluid flow rate

One of the two remaining resistances where thermal gain can be obtained is R_{conv}. Two ways to reduce this resistance are possible, which are to increase A or h_{micro}. From equations (6), (9) and (10), it can be concluded that for a same cross-section area and flow rate, higher aspect ratio channels increases h_{micro}. Furthermore, both A and h_{micro} can be raised by increasing n and adjusting w_{chan} so that the total microchannels width $w_{chan}*n$ is kept constant. Fig. 12 shows a linear correlation with the maximum power over the evaluated range of n at a constant flow rate of 0.75 cm³/s.

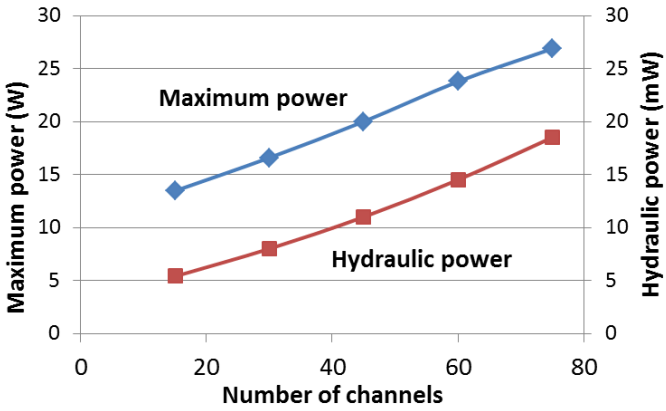

Fig. 12 – Maximum and hydraulic powers admissible microchannels simulation with variable number of microchannels (0.75 cm³/s)

Increasing the number of channels comes at the price of higher accuracy requirements for fabrication and weakened walls due to their reduced width. Another drawback of this approach is the increase of ΔP in the microchannels. So, the price for this solution is paid in pumping power. The ΔP for the related number of microchannels and at the reference flow rate is presented in Table 4.

From Fig. 10, one can observe that the heat flux extracted from the microchannels is limited to the vicinity of the heat sources. This means that the apparent A and $\dot{V}$ are much reduced compared to the real A and $\dot{V}$. By extension, to decrease the apparent R_{heat} and R_{conv}, the Si die should be thickened. According to the results presented on Fig. 13, doubling the bulk thickness from 75 to 150 µm raises the maximum allowed power of 4.2 W, which represents 17.6 % power increase compared to the baseline configuration. Such a solution is however restricted to standalone chip, as the die thickness in 3D chips are generally limited due to the presence of TSVs.

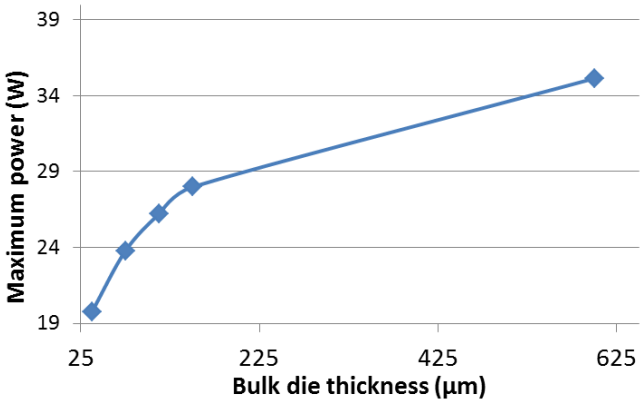

Fig. 13 - Maximum power admissible according to bulk die thickness

Table 4 – Fluidic properties in the different simulations

Flow rate (cm³/s)	n	w_{chan} (µm)	Re	L_c (%)	ΔP (kPa)	P_h (mW)
0.375	60	75	13.8	1.3	9.7	3.6
0.75	60	75	27.6	2.6	19.3	14.5
1.5	60	75	55.2	5.1	38.7	58.1
3.75	60	75	138.1	12.7	96.7	362.6
7.5	60	75	276.1	25.5	193.3	1 449.8
0.75	15	300	52.0	7.2	7.2	5.4
0.75	30	150	40.2	4.8	10.7	8.0
0.75	45	100	32.7	3.4	14.7	11.0
0.75	75	60	23.9	2.0	24.7	18.5

Another strategy to increase the maximum power in the observed ranges is to increase the number of microchannels before increasing the flow rate. The gain in chip power per ΔP is approximately of 0.56 W/kPa when increasing the number of channels and is of 0.3 W/kPa when changing the flow rate between 0.375 and 0.75 cm³/s, decreasing further as the flow rate increases. So, more gains are made by increasing the amount of microchannels than increasing the fluid flow rate.

3D chip application

When transposing the baseline microchannels configuration from the standalone chip to the 3D chip, only R_{cond} and the heat spreading are affected. The total bulk Si, excluding the microchannels depth, passes from 75 µm to 155 µm thick if the two dies are included, raising the space for heat spreading significantly. However, the added interdie polymer layer thermal resistance acts as a bottleneck, forcing the heat flux to spread wide in the Si die rather than to directly cross the polymer layer. Although its presence makes the heat

to spread in the Si die layer, such resistance is detrimental to R_{tot} as its own contribution to spreading is low compared to its added series resistance. In such case, the spreading observed in the die is an answer from the heat flux to exploit at best the parallel and series resistances to cross the polymer layer.

The simulation, presented in Fig. 14, gave a maximum temperature of 129 °C for 16 W, meaning R_{tot}=5.9 °C/W and a maximum power of only 15.3 W, representing a loss of 36 % from the allowed power in the baseline standalone chip. This denotes that this 3D chip configuration introduces a significant resistive element detrimental for such cooling approach.

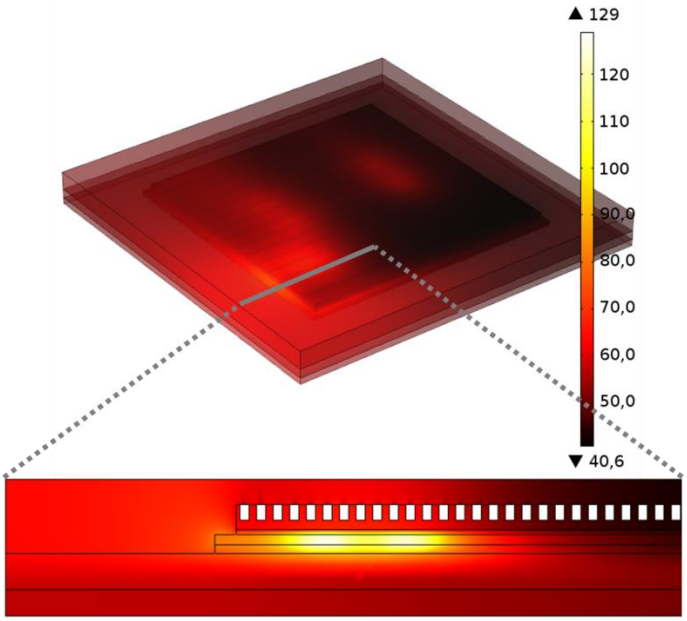

Fig. 14 – Thermal simulation for 3D stacked chip dissipating 16 W (0.75 cm³/s)

The much higher R_{tot} from the 3D stacked model comes from the interdie underfill layer. Fig. 14 clearly shows that the temperature drops when crossing this layer. This implies that when this kind of 3D stack set up is considered, R_{cond} becomes dominant and the focus should be put to reduce this resistance.

Two solutions are suggested, whether to implant the microchannels elsewhere in order to avoid the underfill layer in the heat path or to reduce the underfill resistance. The first solution could be achieved, for example, by moving the microchannels in the bottom die while the second solution could be achieved by integrating thermally conductive material in the underfill layer for the region just above the hotspot. Thereof, the challenges to reduce the total thermal resistance can be completely different for a standalone chip versus a 3D stack configuration.

The interdie resistance can be significantly reduced by introducing Cu micro-pillars in the interdie underfill layer over the heat sources, even if electrical connections are not required. Such addition can increase the thermal conductivity up to 15.8 W/m-K in the normal direction and to 3.8 W/m-K in the planar direction, as obtained by Souare *et al.* [21]. A simulation proposing a uniform micropillars distribution on the whole layer is presented in Fig. 15. In such context, the maximum temperature drops to 95.8 °C, allowing 24.4 W, which is similar to the standalone chip configuration. This confirms that the increased conduction resistance coming from the 3D chip configuration can be compensated and so, such 3D stacked chips with localized heat sources can be cooled through top die microchannels.

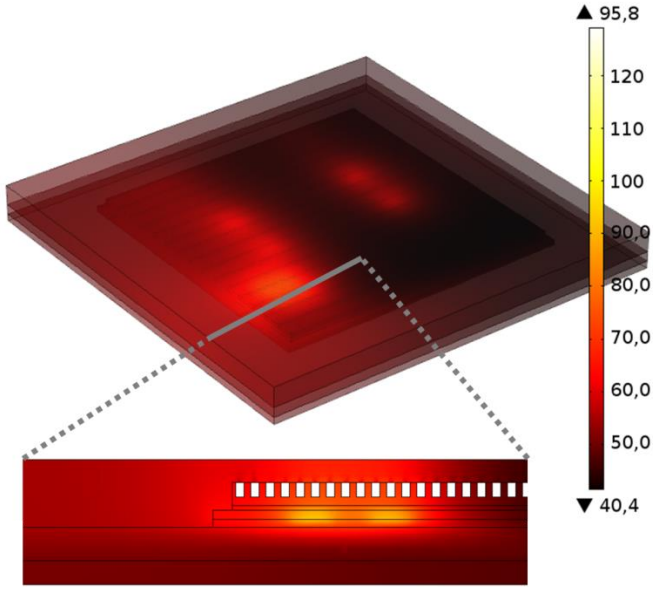

Fig. 15 - Thermal simulation for 3D stacked chip dissipating 16 W with micropillars embedded interdie underfill (normal and lateral thermal conductivities of respectively 15.8 and 3.8 W/m-K; flow rate of 0.75 cm³/s)

CONCLUSION

The goal of this work was to investigate microchannels design parameters in order to establish some design opportunities. It was accomplished through a simulation model integrating analytical microfluidic relations with a FEM of conduction in a microelectronic chip. It uses an iterative approach where heat fluxes on microchannel walls and fluid temperature are analytically calculated and integrated to the simulation. Since the FEM tool is based on commercial software, it offers a potential design tool for subsequent multiphysics simulations, such as thermomechanical, or advanced post-processing tools. The model also integrates elements such as TSVs through homogenized layer zones.

A standalone chip was first used as a baseline case study, where the flow rate and the number of microchannels at constant total cross-section area were investigated. Increasing the flow rate reduced the total resistance, although its impact reached an asymptote as its value increased. On the other hand, the number of microchannels linearly increased the maximum chip power allowable, showing no asymptotic effect in the observed range. Finally, increasing the Si thickness also presented significant increase in the maximum available power. Results suggest that for similar set ups and in the range and configuration observed, increasing the number of channels or die bulk thickness could be more efficient ways to use extra

pressure drop than increasing fluid flow. A second model representing a 3D stacked chip showed that the interdie underfill layer can act as a thermal barrier, which would significantly reduce the allowable chip power in the case of localized heat sources. However, if the underfill thermal conductivity in the thickness axis is increased using non-electronic Cu micropillars through the whole interdie layer, this thermal barrier is significantly reduced. Such approach allowed the 2 dies stacked chip to reduce its total thermal resistance to a value comparable to the standalone chip. This predominant conduction thermal resistance in 3D chips completely changes the strategy to reduce the total thermal resistance relatively to standalone configuration.

This study highlighted the relative importance of the three kinds of resistances met in microfluidic chip cooling, and that conventional thinking is challenged when realistic module configurations are considered.

NOMENCLATURE

Acronyms:

3DIC: 3D integrated circuit
BGA: Ball grid array
FEM: Finite element method
PCB: Printed circuit board
TSV: Through silicon via

Variables:

A_{cond}: Apparent surface for heat conduction
A_{conv}: Apparent microchannels surface
C_p: Fluid heat capacity
D_h: Hydraulic diameter
L_e: Microchannel characteristic length
$L_{e\ rel}$: Microchannel characteristic length divided by the total microchannel length
L_{tot}: Mircrochannel length
Nu_∞: Nusselt number in developed flow
P_h: Hydraulic power
$\dot{Q}_{channel}$: Total heat flux from the walls at an iteration *i*
$\dot{Q}_i$: Total heat flux from the walls at an iteration *i*
$\dot{Q}_{sect}$: Incoming heat flux from section walls to fluid
$\dot{Q}_{tot}$: Total heat from heat source
Re: Reynolds number
R_{cond}: Thermal resistance through chip layers
R_{heat}: Thermal resistance equivalent to temperature rise
R_{tot}: Total thermal resistance of the heat path
T: Temperature
T_{fluid}: Discrete fluid temperature in a microchannel
T_{inlet}: Microchannel inlet temperature
T_{inter}: Microchannel temperature between sections
T_{max}: Maximum temperature in the chip
T_{outlet}: Microchannel inlet temperature
T_{sect}: Fluid average temperature in a section
T_{source}: Source temperature
T_{wall}: Wall temperature
$\dot{V}$: Fluid flow rate
V_{avg}: Average flow speed
f: Darcy friction factor
h_{bot}: Convection coefficient below the chip
h_c: Microchannels depth
h_{micro}: Convection coefficient on microchannels walls
h_{surr}: Convection coefficient around and above the chip
i: Iteration number
k_f: Fluid thermal conductivity
lim: Heat flux convergence criterion
n: Section number
w_c: Microchannels width
α: Largest form factor between w_{chan}/h_{chan} and h_{chan}/w_{chan}
μ: Dynamic viscosity
ρ: Fluid density

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